Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.019”**

**.019”**

**.0054”**

**.0048”**

**.0032”**

**.0032”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: (See Above)**

**Backside Potential: Collector**

**Mask Ref: TVO**

**APPROVED BY: DK DIE SIZE .019” X .019” DATE: 9/29/22**

**MFG: ALLEGRO / SPRAGUE THICKNESS .006” P/N: 2N3904**

**DG 10.1.2**

#### Rev B, 7/19/02